EMU Peripheral Crate Controller

Data Formats

Warning: The contents of this document are preliminary and are subject to change without notice!

Rev. 1.13

Document Rev.	Document Date	Firmware Rev.	Firmware Date	Changes
1.01	6/29/2005			Fixed typoes in examples page (in VME control word).
1.02	7/8/2005	2.18	7/8/2005	Added new function codes and return data types corresponding to firmware version 2.18.
1.03	7/12/2005			Note that function codes 0x05 - 0x16, 0x21, and 0x23 are not yet implemented. Also return data header formats are not yet implemented as shown in this document.
1.04	9/29/2005	3.06	8/31/2005	Return data header format in firmware revision 3.06 and later now matches the format described in this document (except AK/Status codes are not yet implemented). Flash memory functions added (0x05 - 0x16). Separate path for spontaneous packets now implemented (Errors, Warnings, Info, and Interrupts) although interrupt handling is not yet implemented.
1.05	10/26/2005	3.06	8/31/2005	Configuration register bits specified; Restriction on MAC addresses detailed.
1.06	11/15/2005	3.09	11/1/2005	Added error handling in VME master for bus errors (BERR); Packet type codes for INFO/WARN/ERR and INTR has changed; defined a format for identifying INFO/WARN/ERR sources;
1.07	11/15/2005	3.11	11/8/2005	Added interrupt handler module; Changed VME_config register definitions and defaults.
1.08	11/16/2005	3.12	11/16/2005	Added functions for writing and reading serial numbers to/from FLASH
1.09	3/22/2006	3.55	3/8/2006	Improved error handling; Redefined INFO/WARN/ERR formats; Extensively tested and tweaked VME interface to make it less sensitive to backplane noise and glitches; Added Wrt_CR_ID (write Cnfg reg. based on ID) function; Redefined front panel switch 2; Added BOD (Beginning Of Data) marking in external FIFO to separate packets of VME data to facilitate error recovery; Changed slow clock generation method to utilize SRLs (area efficient); Optimized some areas of VME interface to improve timing issues.
1.10	8/4/2006	3.59	5/4/2006	Corrected VME configuration register's firmware defaults and added the power on configuration as shipped for all configuration registers.
1.11	1/15/2008	4.28	1/9/2008	New header format, function codes added and changed, new return packet types added , JTAG interface data formats, universal error code formats, and new configuration register bits defined.
1.12	2/8/2008	4.2B	2/8/2008	Additional universal code words for external FIFO module.
1.13	2/15/2008	4.3	2/13/2008	Added Ack/Status definition table; active internal links indicated in blue rectangles.

Ethernet Packet Format

Mnemonic	Meaning	Size (bytes)	Code/Value
SOP	Start of Packet	1	0xFB
Preamble	Bit patttern for synchronization.	7	6(0x55)(0xD5)
SOF	Start of Frame (last byte of preamble)	1	0xD5
MAC Dest.	Destination MAC address	6	Hardware Defined
MAC Src.	Source MAC address	6	Hardware Defined
LEN	Length of User Data in bytes	2	2-9000
User Data	User specified data	46-9000	User defined
CRC	Cyclical Redundency Check	4	Packet defined
EOP	End of Packet	1	0xFD

User Data Format

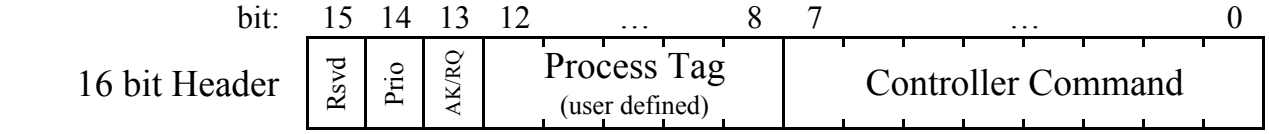
There are 3 general user data formats for the following 3 cases:

1) Packets sent to the controller.
2) Packets returning from the controller (with PROTOCOL disabled).
3) Packets returning from the controller (with PROTOCOL enabled).

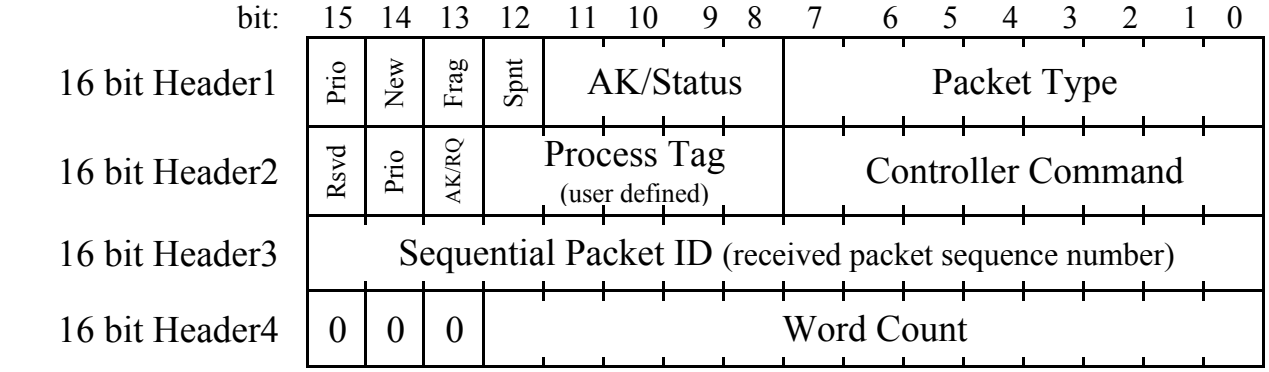
Sequence (16 bit words)	Sent to	Received from (PROTOCOL disabled)	Received from (PROTOCOL enabled)
0	Header	Command Dependent Data	Header1
1	Command Dependent Data	Command Dependent Data	Header2
2	Command Dependent Data	Command Dependent Data	Header3
3	Command Dependent Data	.	Header4
4	.	.	Command Dependent Data
5	.	.	Command Dependent Data
6	.	.	Command Dependent Data
.	.	.	.
.	.	.	.
.	.	.	.

Header Formats

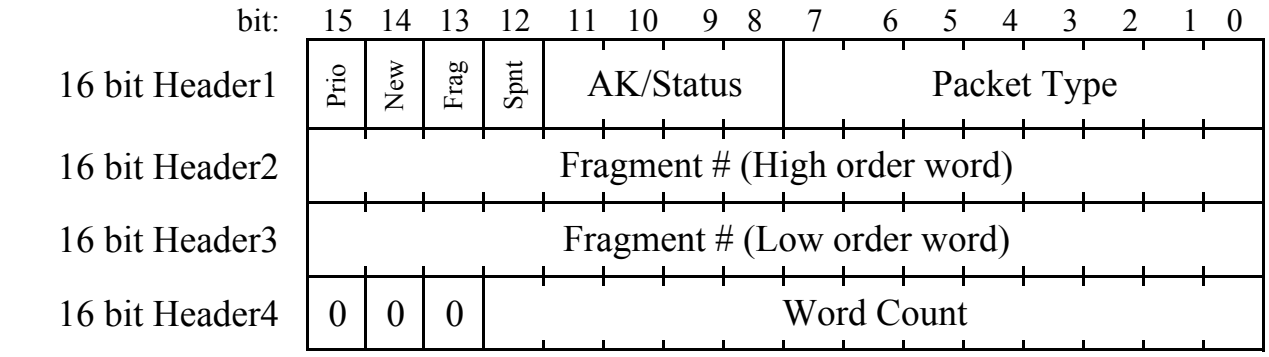
For packets sent to the controller:



For new packets retruned from the controller:



For continued packet fragments retruned from the controller:



Definitions of labels and abbreviations

Rsvd.	:	Reserved.
Prio.	:	Priority packet. To be executed or returned out of sequence ASAP.
AK/RQ	:	Acknowledgement of command execution is requested.
Process Tag	:	Used to identify the process that sent the command.
Controller Command	:	Function code to be executed: Data format is dependent upon this code.
New	:	Indicates that this is the first packet in a series of 1 or more packets.
Frag.	:	Indicates that the amount of data exceeds the maximum packet size. This packet contains only a fragment of the requested data.
Spnt.	:	Indicates that this packet was spontaneously generated by the controller and was not in response to a request.
AK/Status	:	Acknowledgement status. Indicates disposition of the requested function.
Packet Type	:	Indicates the type of data contained in this packet. The data format is dependent upon this type.
Sequential Packet ID	:	A 32 bit number specifying the order in which the packet was received.
Fragment #	:	A 32 bit number specifying this packets position in a sequence of packet fragments.
Word Count	:	The number of data words to follow the header.

Function Codes

Cat.	Mnemonic	OpCode	Functional Description	Data Format
Initialization/Configuration	Funct_NoOp	0x00	No action taken.	no data
	Set_FF_Test	0x01	Set test mode for external FIFO.	no data
	Set_FF_VME	0x02	Set VME mode for external FIFO.	no data
	ECC_enable	0x03	Enable Error Correcting Codes in external FIFO	no data
	ECC_disable	0x04	Disable Error Correcting Codes in external FIFO	no data
	Save_Cnfg_Num	0x05	Save current controller configuration as specified configuration number.	1 word
	Read_Cnfg_Num_Dir	0x06	Direct readback of specified stored configuration (raw data from Flash mem).	1 word
	Read_Cnfg_Num_Dcd	0x07	Decoded readback of specified stored configuration.	1 word
	Rstr_Cnfg_Num	0x08	Restore controller configuration to specified configuration.	1 word
	Set_Cnfg_Dflt	0x09	Set default controller configuration to specified number.	1 word
	Read_Cnfg_Dflt	0x0A	Readback the default configuration number.	no data
	Set_MACs	0x0B	Set MAC addresses.	MAC_FMT[1]
	Read_MACs_Dir	0x0C	Direct readback of stored MAC addresses (raw data from Flash mem).	no data
	Read_MACs_Dcd	0x0D	Decoded readback of stored MAC addresses.	no data
	Read_CRs	0x0E	Readback configuration registers (CR's).	no data
	Wrt_Eth_CR	0x0F	Write Ethernet CR with specified data.	1 word
	Wrt_Ext_CR	0x10	Write External FIFO CR with specified data.	1 word
	Wrt_Rst_CR	0x11	Write reset enables CR with specified data.	1 word
	Wrt_VME_CR	0x12	Write VME CR with specified data.	1 longword[2]
	Wrt_BTO_CR	0x13	Set VME Bus Timeout to specified data.	1 word
	Wrt_BGTO_CR	0x14	Set VME BusGrant Timeout to specified	1 word
	Wrt_All_CRs	0x15	Write all CR's and timeouts with specified	CR_FMT[1]
	Set_Clr_CRs	0x16	Set or Clear individual bits of a CR.	Set_Clr_FMT[1]
	Set_Inj_Err	0x17	Enable error injecting into FIFO data bits	no data
	Rst_Inj_Err	0x18	Disable error injecting into FIFO data bits	no data
	Warn_On_Shdwn	0x19	Enable warning packets prio to reloading.	no data
	No_Warn_On_Shdwn	0x1A	Disable warning packet on shutdown.	no data
	Snd_Startup_Pkt	0x1B	Enables sending an INFO packet on start-up.	no data
	No_Startup_Pkt	0x1C	Disables sending start-up INFO packets.	no data
	Wrt_Ser_Num	0x1D	Write 24-bit PCB serial number.	1 longword[2]
	Rd_Ser_Num	0x1E	Read 24-bit PCB serial number.	1 longword[2]
	Wrt_CR_ID	0x1F	Write CR(s) and timeout(s) to reg. ID	CR_ID_FMT[1]

Function Codes Continued

Cat.	Mnemonic	OpCode	Functional Description	Data Format
VME functions	VME_Cmds	0x20	Specified data are VME commands and are sent through external FIFO.	VME_DAT_FMT[1]
		0x21	Undefined	
	VME_Dir_Cmds	0x22	Specified data are VME commands and are sent directly to VME interface.	VME_DAT_FMT[1]
		0x23	Undefined	
		0x24	Undefined	--
		.	Undefined	--
		.	Undefined	--
		.	Undefined	--
		0x2F	Undefined	--
JTAG	Rd_Dev_ID	0x30	Read device ID from PROM	no data
	Rd_User_Code	0x31	Read user code from PROM	no data
	Rd_Cust_Code	0x32	Read customer code from PROM	no data
	Rd_Back_PROM	0x33	Readback PROM data	no data
	Erase_PROM	0x34	Erase PROM	no data
	Program_PROM	0x35	Program PROM	no data
	Reload_FPGA	0x36	Load FPGA from PROM using PROM cf	no data
	Verify_PROM	0x37	Verify PROM	no data
	Chk_JTAG_Conn	0x38	Check for a working JTAG path.	no data
	Exec_Routine	0x39	Execute the specified routine	1 word
	Ld_Rtn_Base_Addr	0x3A	Load the specified base address for	1 word
	Module_Status	0x3B	Get the JTAG module status	no data
	Write_JTAG_FIFO	0x3C	Write data into the JTAG buffer (16k words)	N words[3]
	Write_Prg_Space	0x3D	Write program data into the program RAM	N words[3]
	Read_Prg_Space	0x3E	Readback the current routine from RAM	no data
	Abort_JTAG_Cmnds	0x3F	Abort JTAG commands and flush buffer.	no data
Flash Direct	Flash_R_W	0x40	Read or Write Flash memory. Data contains commands for Flash interface.	FLASH_FMT[1]
		.	Undefined	--
		.	Undefined	--
		.	Undefined	--
		0xDF	Undefined	--
Undefined		0x50	Undefined	--
		.	Undefined	--
		.	Undefined	--
		.	Undefined	--
		0xDF	Undefined	--

Function Codes Continued

Cat.	Mnemonic	OpCode	Functional Description	Data Format
External FIFO Testing and Programming	Wrt_Ext_FF	0xE0	Write specified data to external FIFO.	N words[3]
	Prg_Ext_Off	0xE1	Program offsets for external FIFO. (18-bit full offset, then 18-bit empty offset)	2 longwords[2,4]
	Rdbk_Ext_Off	0xE2	Readback offsets from external FIFO.	no data
	PRst_Ext_FF	0xE3	Partial reset of external FIFO.	no data
	Rd_Ext_FF	0xE4	Read specified number of words from external FIFO.	1 longword[2]
	RT_Ext_FF	0xE5	Retransmit specified number of words from external FIFO.	1 longword[2]
	MRst_Ext_FF	0xE6	Master reset of external FIFO.	no data
	ST_MK_Ext_FF	0xE7	Set MARK at current read pointer location.	no data
	RST_MK_Ext_FF	0xE8	Reset MARK; restore normal operation	no data
	Rst_Ext_Err_Cnt	0xE9	Reset FIFO data bit error counters.	no data
	Rd_Ext_Err_Cnts	0xEA	Readback FIFO data bit error counters.	no data
		0xEB	Undefined	--
		.	Undefined	--
		.	Undefined	--
		.	Undefined	--
	Flush_2_BOD	0xEF	Flush FIFO to "Beginning Of Data" marker	--
Test and Diagnostic	Rst_Seq_ID	0xF0	Reset sequential packet ID to zero.	--
		.	Undefined	--
		.	Undefined	--
		.	Undefined	--
	Force_Reload	0xF9	Force reprogramming the FPGA.	no data
		.	Undefined	--
		.	Undefined	--
		.	Undefined	--
	Send_N_Words	0xFD	Request specified number of words be sent from the controller.	1 longword[2]
	Load_User_Reg	0xFE	Load the 32 bit LED user register with specified data.	1 longword[2]
	Loopback	0xFF	Transmit the data in this packet back to sender as is.	N words[3]

[1]See section on "Function Specific Sub Formats" for details on specified data format.

[2]High order word sent first, with unused high order bits padded with zeros.

[3]The number of words are defined by LEN in the MAC frame header.

[4]Two words for the FULL offset come first followed by two words for the EMPTY offset.

Function Specific Sub Formats

(After Header)

MAC_FMT (function: Set_MACs; OpCode 0x0B)

MAC_ID ≤ 4:

Sequence (16-bit Words)

	bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	MAC_ID*			
1	Octet 0								Octet 1							
2	Octet 2								Octet 3							
3	Octet 4								Octet 5							

MAC addr.

*MAC_ID	Name	Use
0	Device	MAC address of device being configured.
1	Mcast1	Group MAC address 1 for multicast packets.
2	Mcast2	Group MAC address 2 for multicast packets.
3	Mcast3	Group MAC address 3 for multicast packets.
4	Dflt_Server	MAC address of default server for spontaneous packets sent from the
5 - 7	-	Not defined.
8	All	Refers to all MAC registers.
9 - 15	-	Not defined.

MAC_ID = 8:

Sequence (16-bit Words)

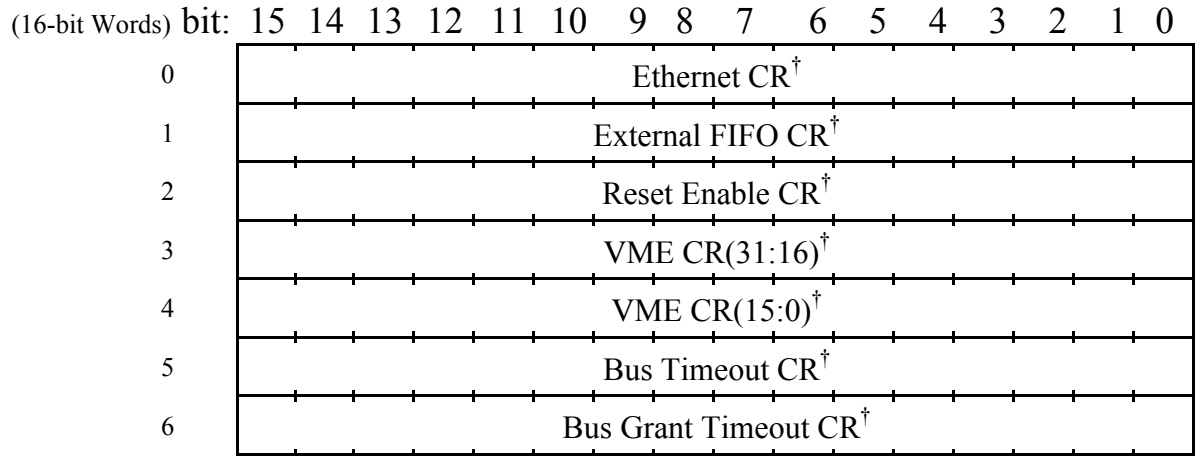
	bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	MAC_ID			
1	Octet 0								Octet 1							
2	Octet 2								Octet 3							
3	Octet 4								Octet 5							
4	Octet 0								Octet 1							
5	Octet 2								Octet 3							
6	Octet 4								Octet 5							
7	Octet 0								Octet 1							
8	Octet 2								Octet 3							
9	Octet 4								Octet 5							
10	Octet 0								Octet 1							
11	Octet 2								Octet 3							
12	Octet 4								Octet 5							
13	Octet 0								Octet 1							
14	Octet 2								Octet 3							
15	Octet 4								Octet 5							

Device | Mcast1 | Mcast2 | Mcast3 | Dflt_Serve

Function Specific Sub Formats (continued)

(After Header)

CR_FMT (function: Wrt_All_CRs; OpCode 0x15)



†See section on "Configuration Register Bits" for details on bit definitions.

Function Specific Sub Formats (continued)

(After Header)

CR_ID_FMT (function: Wrt_CR_ID; OpCode 0x1F)

CR_ID ≤ 5 (except CR_ID = 3):

Sequence (16-bit Words)	bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	CR_ID‡			
1	CR															

CR_ID = 3:

Sequence (16-bit Words)	bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	CR_ID‡			
1	VME CR(31:16)															
2	VME CR(15:0)															

‡CR_ID	CR Name	Use
0	Ethernet	Configuration bits for ethernet module.
1	Ext. FIFO	Configuration bits for external FIFO interfac
2	Reset Ena.	Reset sources and miscelaneous config. bits.
3	VME	Configuration bits for VME interface.
4	BTO	Bus TimeOut in 16 ns units.
5	BGTO	Bus Grant TimeOut in 16 ns units.
6,7	-	Not defined.
8	All	Refers to all CR registers.
9 - 15	-	Not defined.

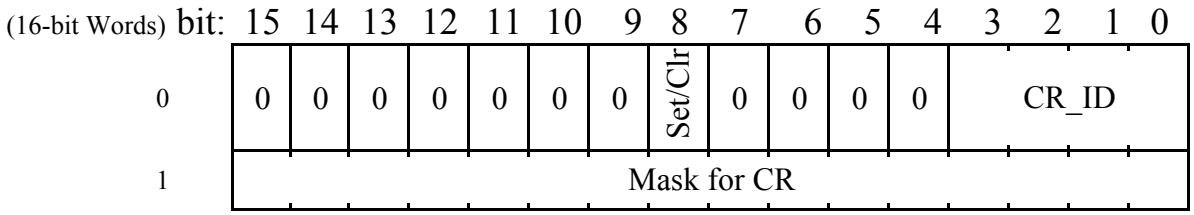
CR_ID = 8:

Sequence (16-bit Words)	bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	CR_ID			
1	Ethernet CR															
2	External FIFO CR															
3	Reset Enable CR															
4	VME CR(31:16)															
5	VME CR(15:0)															
6	Bus Timeout CR															
7	Bus Grant Timeout CR															

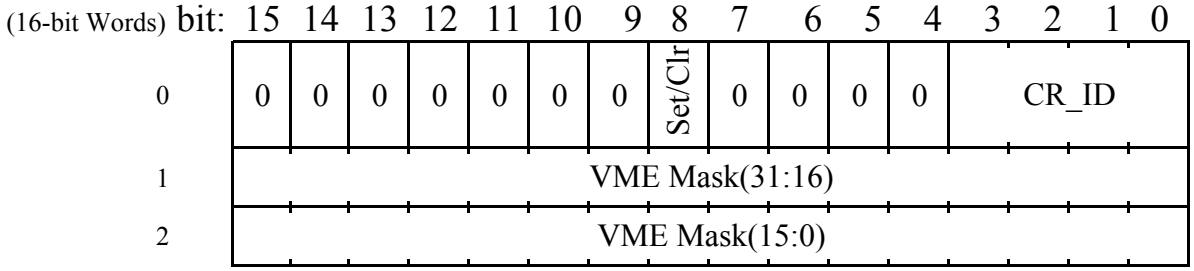
Function Specific Sub Formats (continued)
(After Header)

Set_Clr_FMT (function: Set_Clr_CRs; OpCode 0x16)

CR_ID ≤ 2:



CR_ID = 3:

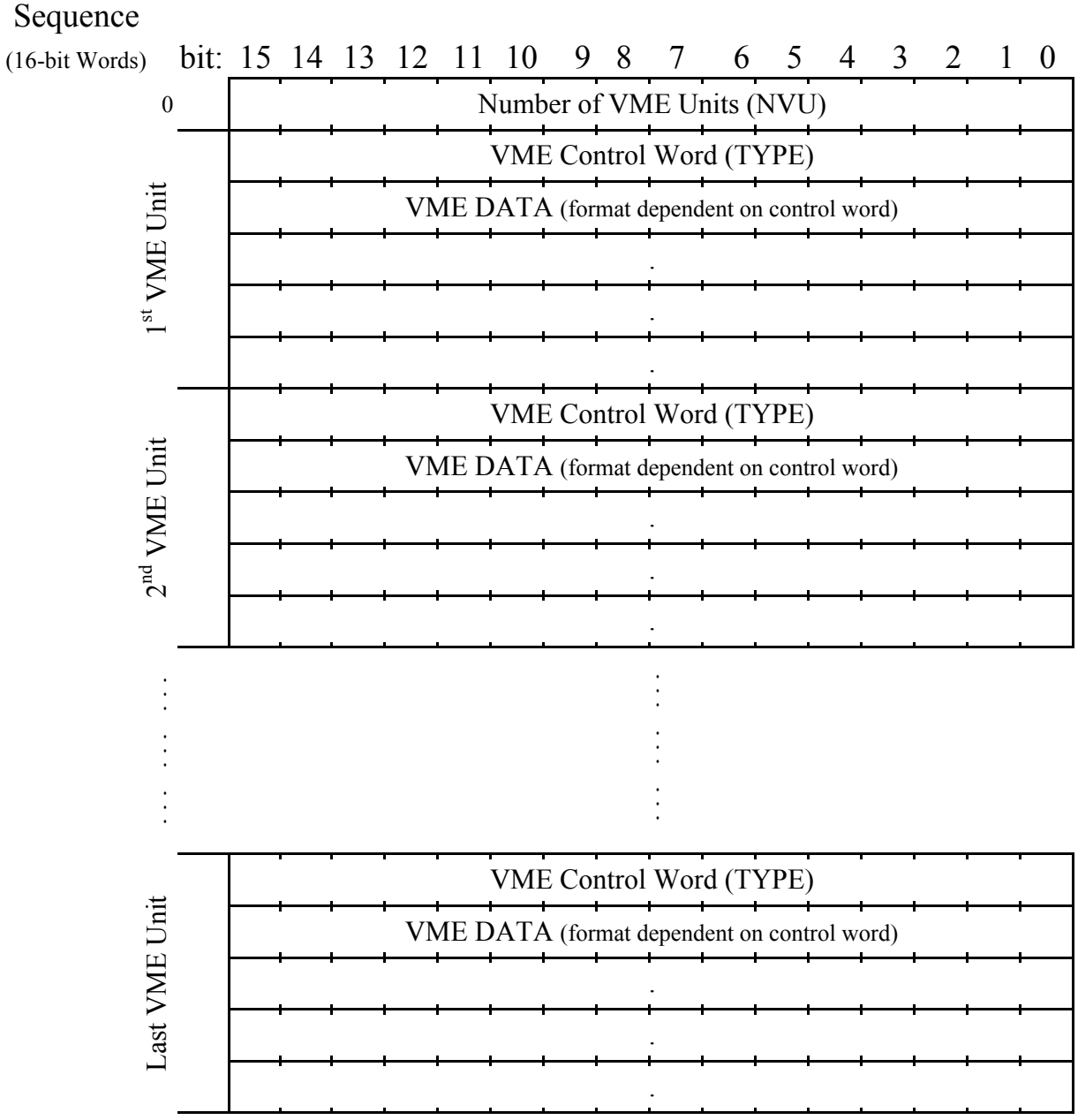


Set/Clr bit	Function
0	Mask is "ANDed" with the specified CR
1	Mask is "ORed" with the specified CR

Function Specific Sub Formats (continued)

(After Header)

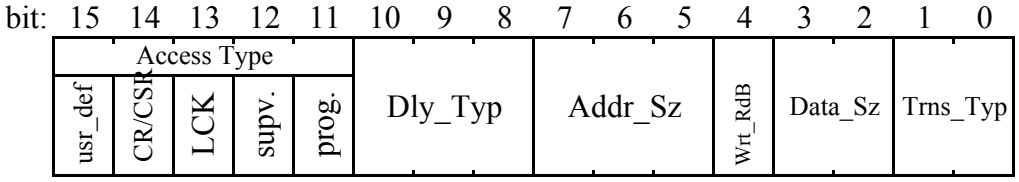
VME_DAT_FMT (function: VME_Cmds; OpCode 0x20 and 0x22)



Function Specific Sub Formats (continued)

(After Header)

VME Control Word



Transfer Types

Trns_Typ Code	Mnem.	Meaning
0	SNGL	Single transfer
1	BLOCK	Block transfer
2	RMW	Read Modify Write sequence
3	UNALG	Unaligned transfer (16-bits crossing word boundries)

Data Sizes

Data_Sz Code	Mnem.	Size	Number of supplied/expected words
0	D08	8 bits	1
1	D16	16 bits	1
2	D32	32 bits	2
3	D64	64 bits	4

Write Control

Wrt_RdB Value	Meaning
0	Read data from specified VME address.
1	Write data to specified VME address

Address Sizes

Addr_Sz Code	Mnem.	Size	Number of supplied/expected words
0	-	-	undefined
1	A16	16 bits	1
2	A24	24 bits	2
3	A32	32 bits	2
4	A40	40 bits	3
5	A64	64 bits	4
6	-	-	undefined
7	-	-	undefined

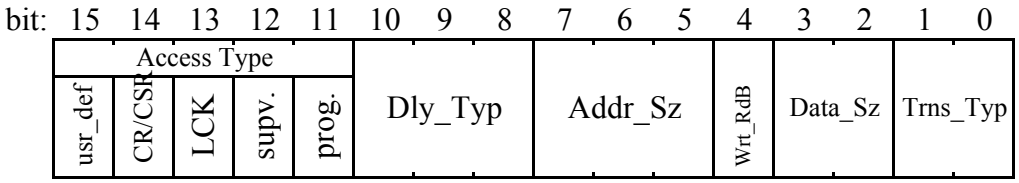
Delay Types

Dly_Typ Code	Mnem.	Clock Period	Num bits	Max Count	Max Delay	Comment
0	No_Dly	-	-	-	-	
1	D4nsX16	4 ns	16	65535	262,144 us	4 ns modes are disabled. If used, 2 bits are dropped and 16 ns clock is used.
2	D16nsX16	16 ns	16	65535	1.049 ms	
3	D16usX16	16.384 us	16	65535	1.074 s	
4	D4nsX32	4 ns	32	4.29E+09	17.18 s	4 ns modes are disabled. If used, 2 bits are dropped and 16 ns clock is used.
5	D16nsX32	16 ns	32	4.29E+09	68.72 s	
6	D16usX32	16.384 us	32	4.29E+09	1.95 hr	
7	undefined	undefined	-	undefined	undefined	

Note: The format of the data following the VME control word is dependent on the options specified in the control word. Please refer to the section on "VME Control Word Dependent Data Format" for the details.

Function Specific Sub Formats (continued)
(After Header)

VME Control Word (continued)



Access Types

Mnem.	Value	Meaning
prog.	0	VME data access
	1	VME program access
supv.	0	non-privledged access
	1	supervisory access
LCK	0	normal transfer
	1	VME Lock command
CR/CSR	0	normal transfer
	1	Config. ROM/Cntrl & Status Reg.
usr_def	0	Standard address modifiers
	1	User defined Address Modifier (UAM)

Note: The format of the data following the VME control word is dependent on the options specified in the control word. Please refer to the section on "VME Control Word Dependent Data Format" for the details.

Function Specific Sub Formats (continued)
(After Header)

VME Control Word Dependent Data Format

General Format of VME Data:

Section / Order	Data Specified	Words	Conditions (data present when…)
Delay Section:	Delay	0,1-2 Words	Dly_Typ ≠ 0
Address Section:	Addr. Mod.	0,1 Words	Dly_Typ = 0 & usr_def = 1
	Address	0,1-4 Words	Dly_Typ = 0
Data Section:	Data Count:	0,1 Word (n)	Dly_Typ = 0 & Trns_Typ = BLOCK
	Data	0-4 Words n-times	Dly_Typ = 0 & Wrt_RdB = 1

Delay Section:

Delay:

	Dly_Typ	
Seq.	D4nsX16 D16nsX16 D16usX16	D4nsX32 D16nsX32 D16usX32
0	Delay(15:0)	Delay(31:16)
1	-	Delay(15:0)

Address Section:

Address Modifier: Specify a user defined address modifier in the range 0x10 to 0x1F;

Address:

	Addr_Sz				
Seq.	A16	A24	A32	A40	A64
0	Addr(15:0)	0x00Addr(23:16)	Addr(31:16)	0x00Addr(39:32)	Addr(63:48)
1	-	Addr(15:0)	Addr(15:0)	Addr(31:16)	Addr(47:32)
2	-	-	-	Addr(15:0)	Addr(31:16)
3	-	-	-	-	Addr(15:0)

Data Section:

Data Count: 16 bit word specifying the number of transfers in the block.

Data:

	Reads	Data_Sz (for writes Wrt_RdB = 1)			
Seq.	Wrt_RdB = 0	D08	D16	D32	D64
0	-	0x00Data(7:0)	Data(15:0)	Data(31:16)	Data(63:48)
1	-	-	-	Data(15:0)	Data(47:32)
2	-	-	-	-	Data(31:16)
3	-	-	-	-	Data(15:0)

Function Specific Sub Formats (continued)

(After Header)

FLASH_FMT (function: Flash_R_W; OpCode 0x40)

Sequence (16-bit Words)	bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	Number of Pages (NP: 1-128)							
1	W[1]	Page Number (0-127)							D[2]	Number of Bytes (NB1: 1-64)						
2	0	0	Byte Address (0-63)						Data							
3	0	0	Byte Address (0-63)						Data							
4	0	0	Byte Address (0-63)						Data							
.	0	0	.						.							
.	0	0	.						.							
.	0	0	.						.							
(NB1+1)+1	W[1]	Page Number (0-127)							D[2]	Number or Bytes (NB2: 1-64)						
(NB1+1)+2	0	0	Byte Address (0-63)						Data							
(NB1+1)+3	0	0	Byte Address (0-63)						Data							
(NB1+1)+4	0	0	Byte Address (0-63)						Data							
.	0	0	.						.							
.	0	0	.						.							
.	0	0	.						.							
NB2+1)+(NB1+1)+1	W[1]	Page Number (0-127)							D[2]	Number or Bytes (NB3: 1-64)						
NB2+1)+(NB1+1)+2	0	0	Byte Address (0-63)						Data							
NB2+1)+(NB1+1)+3	0	0	Byte Address (0-63)						Data							
NB2+1)+(NB1+1)+4	0	0	Byte Address (0-63)						Data							
.	0	0	.						.							
.	0	0	.						.							
.	0	0	.						.							

First Page

Second Page

Third Page

[1]W=1: write to specified page; W=0 : read from specified page.

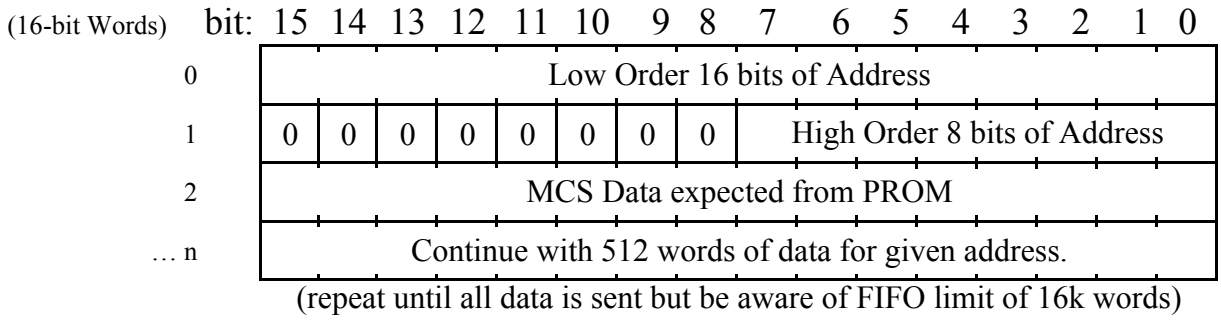
[2]This bit is ignored on writes (W=1). When W=0; D=0 indicates that data is not to be decoded and goes directly to the GbE transmitter; D=1 indicates that data is to be decoded in the configuration module before being sent to the GbE transmitter.

Function Specific Sub Formats (continued)
(After Header)

JTAG_FIFO_FMT (function: Write_JTAG_FIFO; OpCode 0x3C)

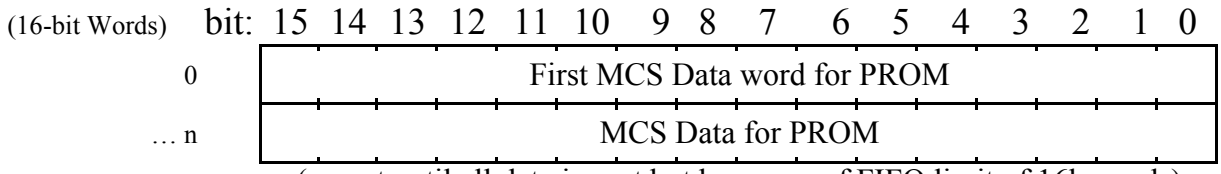
Supply words or bytes as needed based on function being executed.

Case: Sending PROM verification data:



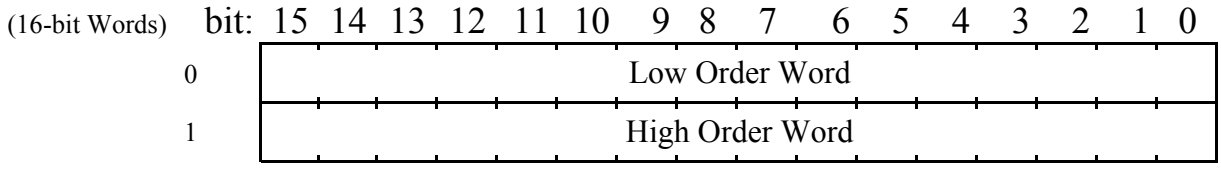
(repeat until all data is sent but be aware of FIFO limit of 16k words)

Case: Sending PROM program data:

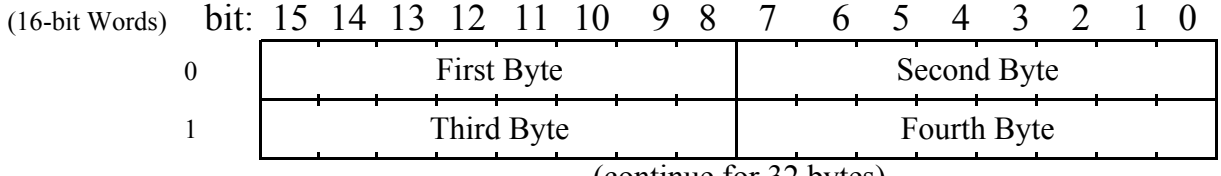


(repeat until all data is sent but be aware of FIFO limit of 16k words)

Case: User Code data:



Case: Customer Code data:

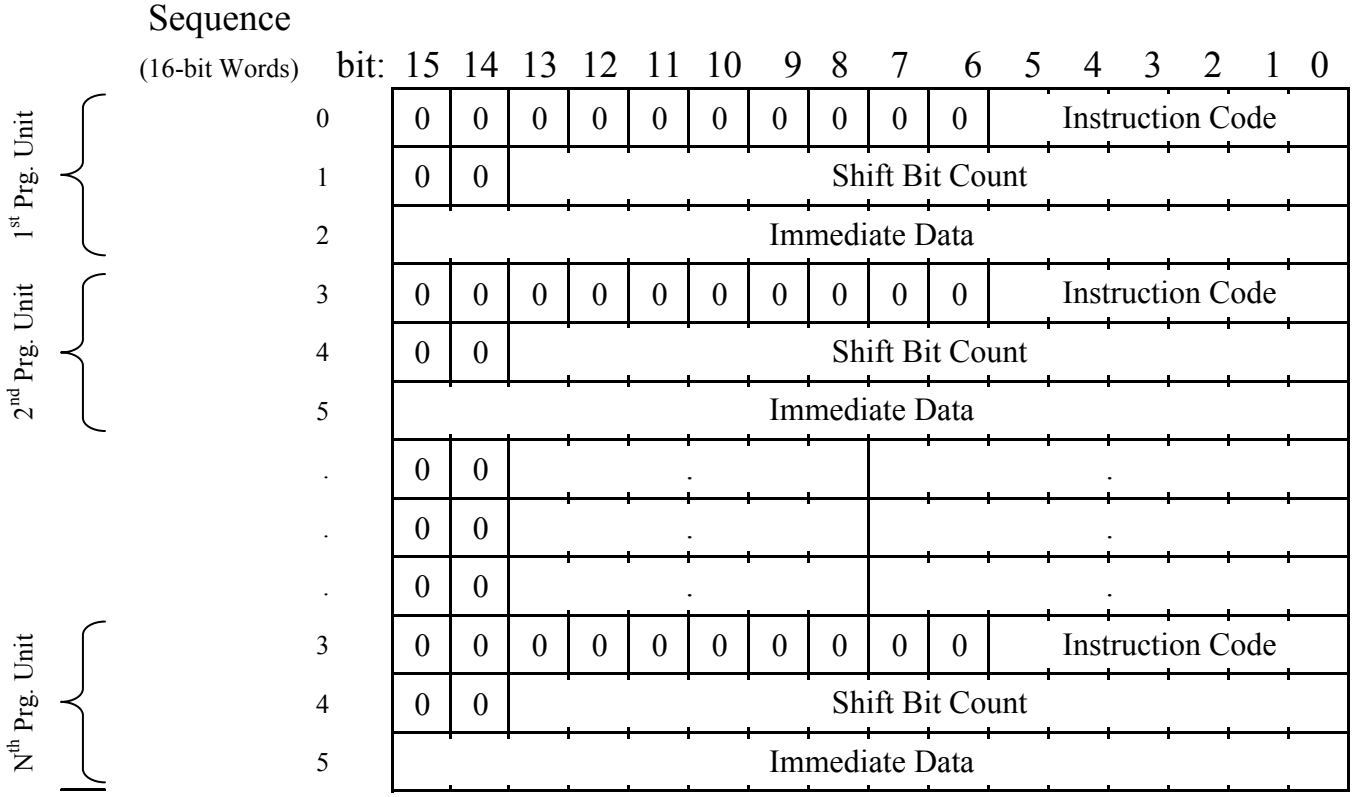


(continue for 32 bytes)

Function Specific Sub Formats (continued)

(After Header)

JTAG_PRG_FMT (function: Write_Prg_Space; OpCode 0x3D)



Return Packet Types

Code	Packet Type		Words per Data Unit
0x00	No data		0
0x01	Loopback data		1
0x02	TX_N_Words requested data		1
0x03	External FIFO data or offsets		mixed[1]
0x04	VME D08 data	Type = {01,Data_Sz} (4+Data_Sz)	1
0x05	VME D16 data		1
0x06	VME D32 data		2
0x07	VME D64 data		4
0x08	JTAG Module data		1
0x09			
0x0A	Configuration Module data		mixed[2]
0x0B	Flash readback data		variable[3]
⋮			
0x10	Ethernet module data		1
⋮			
0xF8	D08 Interrupt packet with 8-bit Status/ID		1
0xF9	D16 Interrupt packet with 16-bit Status/ID		1
0xFA	D32 Interrupt packet with 32-bit Status/ID		2
⋮			
0xFD	Information packet		variable[4]
0xFE	Warning packet		variable[4]
0xFF	Error packet		variable[4]

[1]Dependent on requested data: programed offset (two 18-bit words), error counts (two 32-bit words), or standart FIFO read data (n 16-bit words). (See following pages):

[2]Dependent on requested data: MAC, CR, Serial Num. Etc. (see following pages):

[3]Flash Readback Data Format (see following pages):

[4]For information, warning, and error packets the data format is dependent on the source of the data (see following pages for details):

Acknowledgement/Status Codes

Code	Mnemonic	Data Present	Status
0	No_Ack	No Data After Header	No Acknowledgement Requested or not implemented
1	CC_S		Command Completed Sucessfully
2	CC_W		Command Completed with Warnings
3	CC_E		Command Completed with Errors
4	CE_I		Command Execution finished Incomplete
5	CiP		Command in Progress no warnings no errors
6	CiP_W		Command in Progress with Warnings
7	CiP_E		Command in Progress with Errors
8	No_Ack	Data Present	No Acknowledgement Requested or not implemented
9	CC_S		Command Completed Sucessfully
A	CC_W		Command Completed with Warnings
B	CC_E		Command Completed with Errors
C	CE_I		Command Execution finished Incomplete
D	CiP		Command in Progress no warnings no errors
E	CiP_W		Command in Progress with Warnings
F	CiP_E		Command in Progress with Errors

Return Data Formats

External FIFO Data Format (Packet type 0x03):

Programmed offesets; Response to OpCode 0xE2 (Rdbk_Ext _Off):

Sequence (16-bit Words)

	bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	b17	b16
1	Full Offset(15:0)															
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	b17	b16
3	Empty Offset(15:0)															

Bit error counts; Response to OpCode 0xEA (Rd_Ex _Err_Cnts):

Sequence (16-bit Words)

	bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Count of uncorrected errors—high order word (31:16)															
1	Count of uncorrected errors—low order word (15:0)															
2	Count of corrected errors—high order word (31:16)															
3	Count of corrected errors—low order word (15:0)															

Normal FIFO data; Response to OpCodes 0xE4 or 0xE5 (Rd(T)_Ext _FF):

Sequence (16-bit Words)

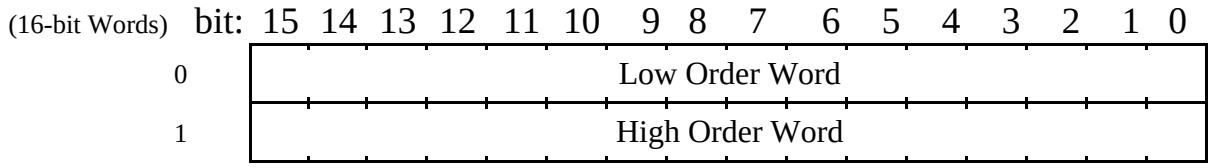
	bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	FIFO contents 1st word (15:0)															
1	FIFO contents 2nd word (15:0)															
2	FIFO contents 3rd word (15:0)															
⋮	⋮															

Return Data Formats (continued)

JTAG Data Readback Format: (Packet type 0x08):

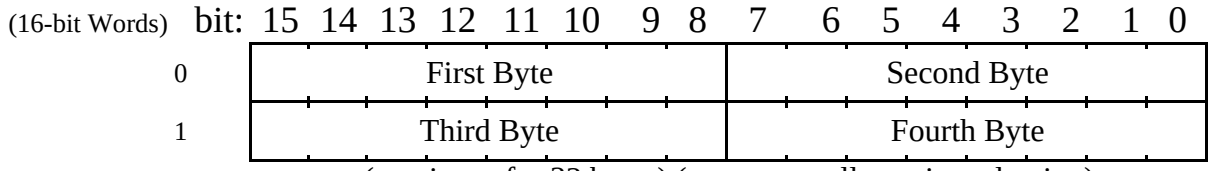
Device ID readback:
Response to OpCode 0x30 or 0x31 (Rd_Dev_ID or Rd_User_Code):

Sequence



Customer Code readback:
Response to OpCode 0x32 (Rd_Cust_Code):

Sequence



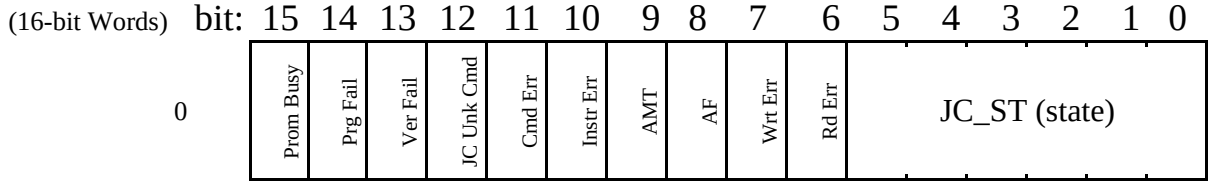
(continues for 32 bytes) (treat as a null terminated string)

PROM Data readback:
Response to OpCode 0x33 (Rd_Back_PROM):

Data is returned as Little Endian short ints, LSB first.

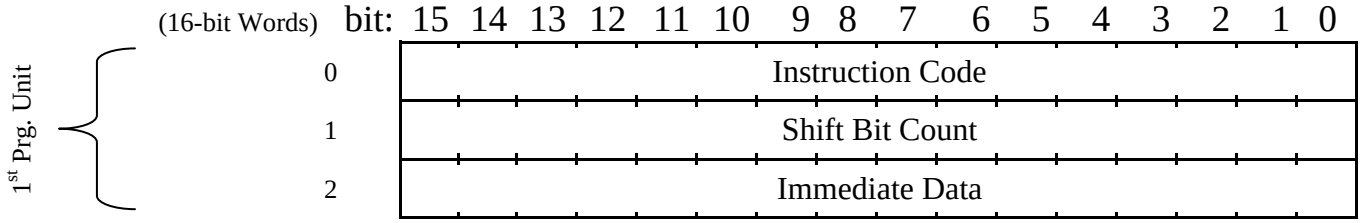
Module Status readback:
Response to OpCode 0x3B (Module_Status):

Sequence



Program Space readback:
Response to OpCode 0x3E (Read_Prg_Space):

Sequence



(repeats until an "End Of Program" is encountered)

Return Data Formats (continued)

Configuration Data Readback Format: (Packet type 0x0A):

Direct read of stored configuration:
Response to OpCode 0x06 (Read_Cnfg_Num _Dir):

Sequence

(16-bit Words)	bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Page							0	Count = 30						
1	0	0	Address						eth_cr(15:8)							
2	0	0	Address						eth_cr(7:0)							
3	0	0	Address						ext_ff_cr(15:8)							
4	0	0	Address						parity_A(11:4)							
5	0	0	Address						parity_A(3:0)				parity_B(11:8)			
6	0	0	Address						parity_B(7:0)							
7	0	0	Address						ext_ff_cr(7:0)							
8	0	0	Address						rst_cr(15:8)							
9	0	0	Address						rst_cr(7:0)							
10	0	0	Address						parity_A(11:4)							
11	0	0	Address						parity_A(3:0)				parity_B(11:8)			
12	0	0	Address						parity_B(7:0)							
13	0	0	Address						vme_cr(31:24)							
14	0	0	Address						vme_cr(23:16)							
15	0	0	Address						vme_cr(15:8)							
16	0	0	Address						parity_A(11:4)							
17	0	0	Address						parity_A(3:0)				parity_B(11:8)			
18	0	0	Address						parity_B(7:0)							
19	0	0	Address						vme_cr(7:0)							
20	0	0	Address						bto_cr(15:8)							
21	0	0	Address						bto_cr(7:0)							
22	0	0	Address						parity_A(11:4)							
23	0	0	Address						parity_A(3:0)				parity_B(11:8)			
24	0	0	Address						parity_B(7:0)							
25	0	0	Address						bgto_cr(15:8)							
26	0	0	Address						bgto_cr(7:0)							
27	0	0	Address						rsvd(15:8)							
28	0	0	Address						parity_A(11:4)							
29	0	0	Address						parity_A(3:0)				parity_B(11:8)			
30	0	0	Address						parity_B(7:0)							

Return Data Formats (continued)

Configuration Data Readback Format: (Packet type 0x0A):

Decoded read of stored configuration or current configuration:
Response to OpCode 0x07 or 0x0E (Read_Cnfg_Num _Dcd or Read_CRs):

Sequence

(16-bit Words)	bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Ethernet CR															
1	External FIFO CR															
2	Reset Enable CR															
3	VME CR(31:16)															
4	VME CR(15:0)															
5	Bus Timeout CR															
6	Bus Grant Timeout CR															

Read default configuration number:
Response to OpCode 0x0A (Read_Cnfg_Dflt):

Sequence

(16-bit Words)	bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	Default Configuration Number							

Read serial number:
Response to OpCode 0x1E (Rd_Ser_Num):

Sequence

(16-bit Words)	bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	SerNo(23:16)							
1	SerNo(15:0)															

Return Data Formats (continued)

Configuration Data Readback Format: (Packet type 0x0A):

Direct read of stored MAC addresses:
Response to OpCode 0x0C (Read_MACs _Dir):

Sequence (16-bit Words)	bit: 15	14	13 12 11 10 9 8	7 6 5 4 3 2 1 0
0	0	Page		0 Count = 60
1	0	0	Address	Octet 0 of Device MAC
2	0	0	Address	Octet 1 of Device MAC
3	0	0	Address	Octet 3 of Device MAC
4	0	0	Address	parity_A(11:4)
5	0	0	Address	parity_A(3:0) | parity_B(11:8)
6	0	0	Address	parity_B(7:0)
7	0	0	Address	Octet 4 of Device MAC
8	0	0	Address	Octet 5 of Device MAC
9	0	0	Address	Octet 6 of Device MAC
10	0	0	Address	parity_A(11:4)
11	0	0	Address	parity_A(3:0) | parity_B(11:8)
12	0	0	Address	parity_B(7:0)
13	0	0	Address	Octet 0 of Mcast1 MAC
14	0	0	Address	Octet 1 of Mcast1 MAC
15	0	0	Address	Octet 3 of Mcast1 MAC
16	0	0	Address	parity_A(11:4)
17	0	0	Address	parity_A(3:0) | parity_B(11:8)
18	0	0	Address	parity_B(7:0)
19	0	0	Address	Octet 4 of Mcast1 MAC
20	0	0	Address	Octet 5 of Mcast1 MAC
21	0	0	Address	Octet 6 of Mcast1 MAC
22	0	0	Address	parity_A(11:4)
23	0	0	Address	parity_A(3:0) | parity_B(11:8)
24	0	0	Address	parity_B(7:0)

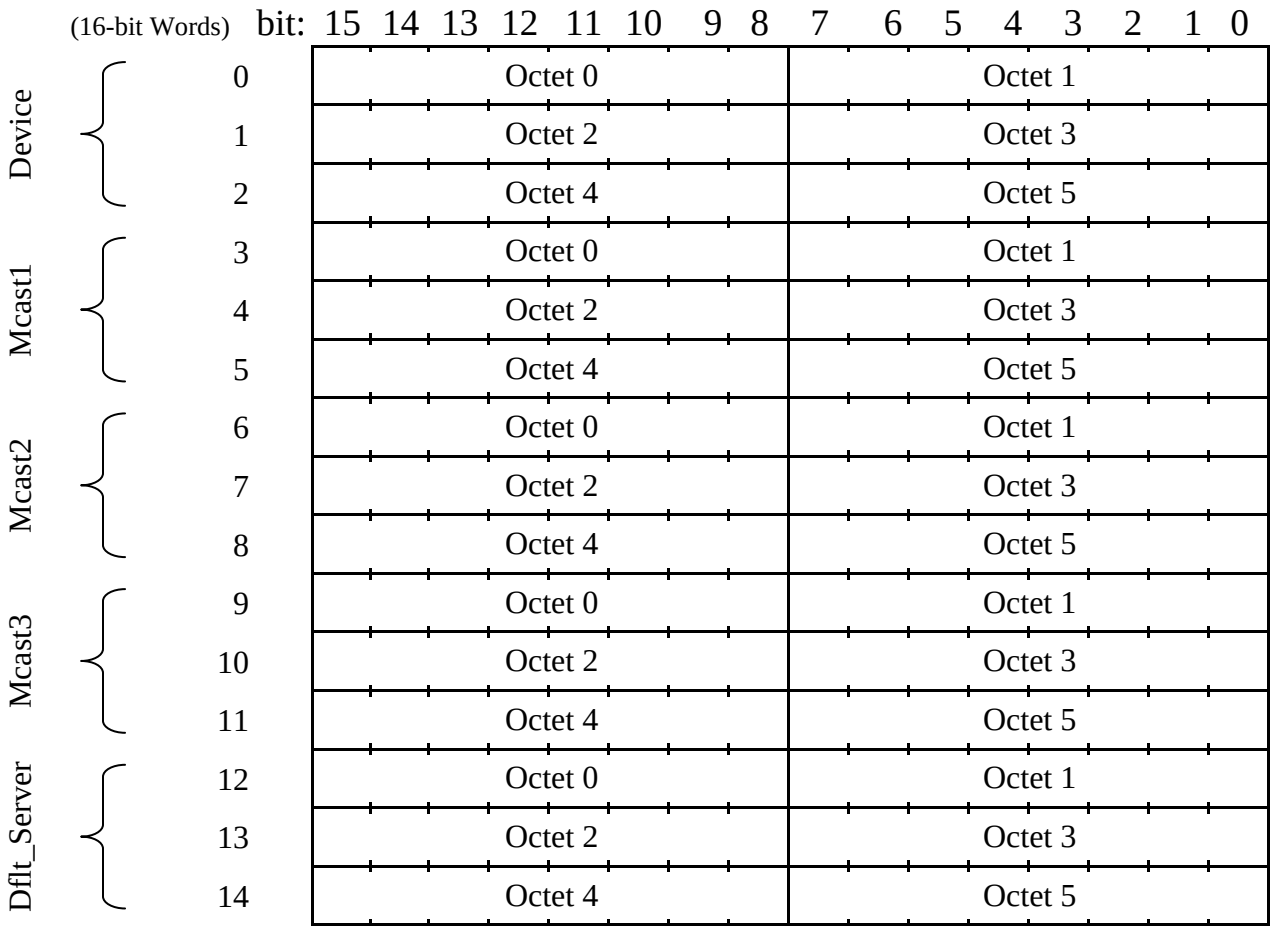
⋮

Pattern repeats for remaining MAC addresses: Mcast2, Mcast3, and Dflt_Server.

Return Data Formats (continued)

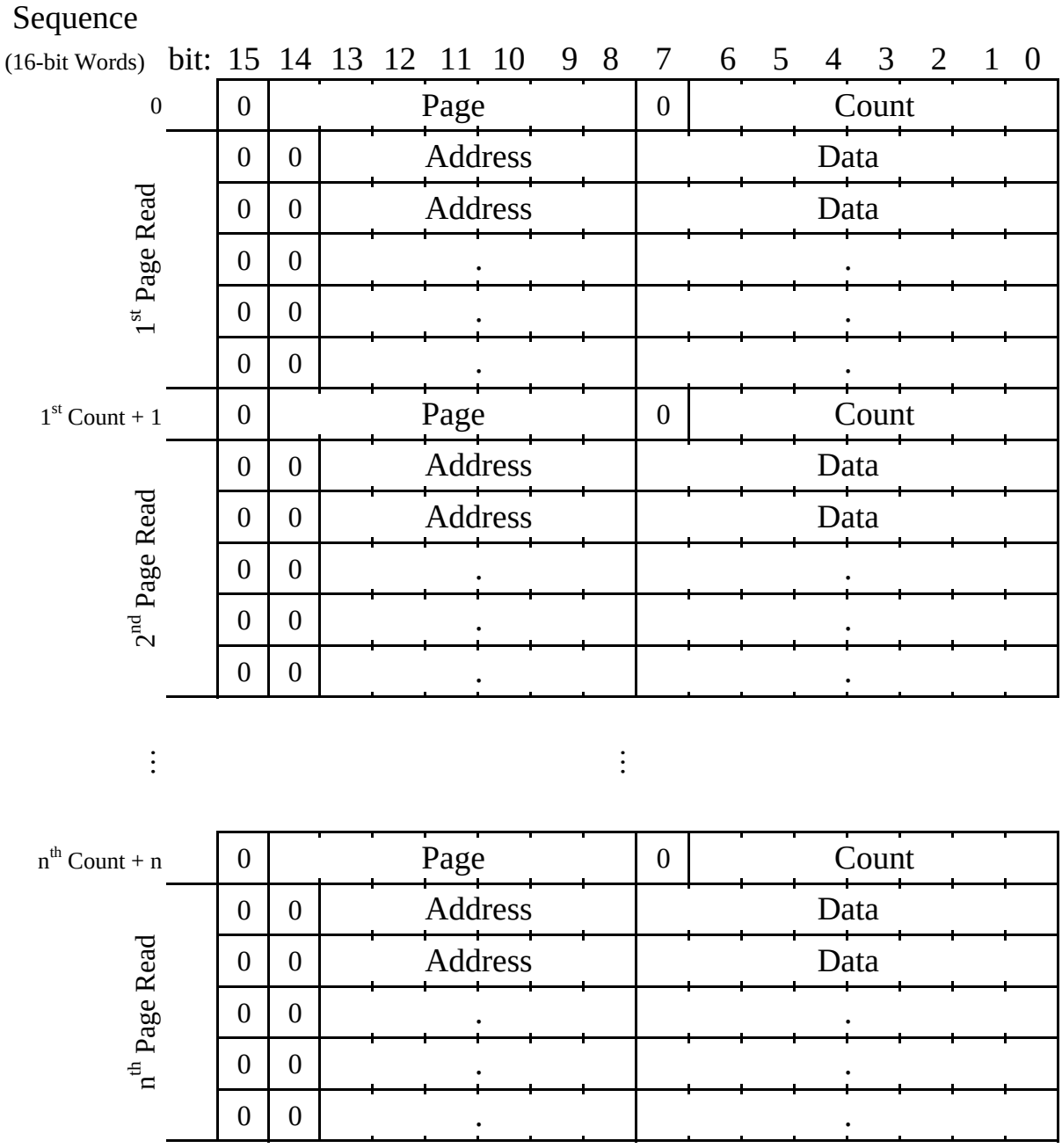
Configuration Data Readback Format: (Packet type 0x0A):

Decoded read of stored MAC addresses:
Response to OpCode 0x0D (Read_MACs _Dcd):



Return Data Formats (continued)

Flash Readback Data Format: (Packet type 0x0B):



Return Data Formats (continued)

Data Format for ERR/WARN/INFO Packet Types

(Packet Types 0xFF, 0xFE, and 0xFD)

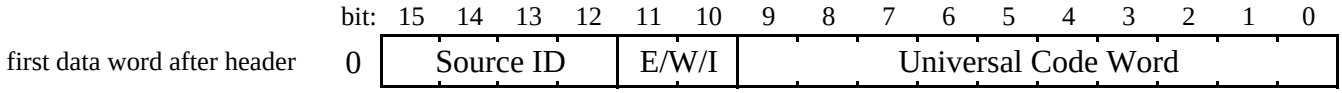


Table of Source ID's

Source ID	Mnemonic	Description
0	Misc.	No specified source
1	VME_Ctrl	VME Controller module
2	VME_Master	VME Master module
3	VME_Rdbk	VME Readback module
4	VME_IH	VME Interrupt module
5	VME_Slv	VME Slave module
6	VME_Arb	VME Arbiter module
7	Ext_FIFO_mod	External FIFO module
8	Eth_Rcv	Ethernet Receive module
9	Eth_Trns	Ethernet Transmit module
10	JTAG_mod	JTAG Interface
11	Flash_mod	Flash module
12	Config_mod	Configuration module
13	BTC_mod	Command Processor module
14	Rst_Hndlr	Reset Handler module
15	Strtup_Shtdwn	Start-up/Shutdown module

Message Type Codes

Code	Mnemonic	Type
0	HDR_Info	Information
1	HDR_Warn	Warning
2	HDR_Error	Error
3	N/A	Not used

Universal Code Words

See appendix A

Return Data Formats (continued)

Data Format for ERR/WARN/INFO Packet Types

(Packet Types 0xFF, 0xFE, and 0xFD)

Additional Words for Specified Message Codes

Codes	Mnemonics	bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
272 - 280	VC_Unkn_Addr VC_Unkown_Dly VC_Incomp_Opt VC_RdEr_Addr VC_RdEr_Dcnt VC_RdEr_Data	1	Access Type: usr_def	CR/CSR	LCK	supv.	prog.	Dly_Typ			Addr_Sz			Wrt_RdB	Data_Sz		Trns_Typ	
288 - 290	VM_BERR_Slv VM_BTO VM_Not_Sup	1	MSTR_ST					AM(5:0)						Wrt_RdB	Data_Sz		Trns_Typ	
		2	High order address word.															
		3	Mid High address word.															
		4	Mid Low address word.															
		5	Low order address word.															
320, 321	VI_BERR_Slv VI_BTO	1	IH_ST				0	Addr			0	IRQ (7:1)						
322	VI_Msk_Chg	1	0	0	0	0	0	0	0	0	0	IRQ Mask						
528	ER_Rcv_Err	1	0	0	0	0	0	0	0	0	0	0	0	Read	Frame Req	MAC Req	FF_Rdy	MT
		2	Frame Length															
560-566	JT_Buf_AF JT_Buf_Ovfl JT_Buf_AMT JT_Buf_RdErr JT_Ukn_Cmd JT_Ver_Fail JT_Prg_Fail	1	Prom Busy	Prg Fail	Ver Fail	JC Unk Cmd	Cmd Err	Instr Err	AMT	AF	Wrt Err	Rd Err	JC_ST					
577-584, 592	FL_In_WtErr FL_In_RdErr FL_TRDS_WtErr FL_TRDS_RdErr FL_PgRd_WtErr FL_PgRd_RdErr FL_ADFF_WtErr FL_ADFF_RdErr CF_Mltp_Flsh	1	0	0	0	0	0	0	0	0	ADFF RdErr	ADFF WtErr	PgRd RdErr	PgRd WtErr	TRDS RdErr	TRDS WtErr	InFF RdErr	InFF WtErr

Examples

Example 1: VME commands for 2 A24D16 single writes, a delay, and then an A24D16 single read.

		Sequence of 16 bit words (HEX)	Meaning
	Header	2020	Function is VME Comands with ackowlegment request
	NVU	0004	Number of VME units
1st VME Unit	Control Word	0054	A24D16 Single Write
	Address	00A(23:16)	High order byte of VME address
		A(15:0)	Low order word of VME address
	Data	D(15:0)	Data word to write
2nd VME Unit	Control Word	0034	A24D16 Single Write
	Address	00A(23:16)	High order byte of VME address
		A(15:0)	Low order word of VME address
	Data	D(15:0)	Data word to write
3rd VME Unit	Control Word	05XX	16 ns by 32 bit delay
	Data	Dly(31:16)	High order word of delay
		Dly(15:0)	Low order word of delay
4th VME Unit	Control Word	0044	A24D16 Single Read
	Address	00A(23:16)	High order byte of VME address
		A(15:0)	Low order word of VME address

Configuration Register Bits:

(Definitions and Defaults)

Ethernet Configuration Register

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Bit definitions	reserved								switch control	spont. pkt ena	carrier extend	protocol enable	promisc.	passthru	tdis	tx inhibit	
Firmware default	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	(0x0050)
Pow-On Cnfg. as Shpd.	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	(0x0050)

switch control : This has been disabled in the firmware. The switch now controls what signals are sent to the test ports for logic analyzer connections.

spont. pkt ena : Enables the controller to send spontaneous packets for errors, warnings, information, and interrupts, otherwise no packets will be sent that are not in response to a request for data. The preferred method of controlling message packets is now Msg_Lvl. See Reset/Misc config register.

carrier extend : For use in half duplex mode at speeds above 100 Mb/s to ensure proper operation of the CSMA/CD protocol (1000 BASE-T).

protocol enable : Specifies whether or not packets sent from the controller are sent with a header. When protocol is enabled, headers are included.

promisc. : Puts controller in promiscuous mode. In this mode the controller accepts all MAC addresses.

passthru : Puts controller in pass-thru mode. In this mode the controller returns the user data portion of all accepted packets received back to the sender without executing any instructions. A header is added if the protocol enable bit is set.

tdis : Disables the transmit side of the optical transceiver. Any established link will be lost. It is suggested that this bit be kept set to zero. This has been disabled.

tx inhibit : Disables the transmit side of the RocketIO™. This prevents Idles from being transmitted and therefore any established link will be lost. It is suggested that this bit be kept set to zero. This has been disabled.

External FIFO Configuration Register

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Bit definitions	reserved													Inject Errors	ECC enable	Test Mode	
Firmware default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	(0x0002)
Pow-On Cnfg. as Shpd.	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	(0x0002)

Inject Errors : Injects errors into data written to the external FIFO for testing ECC function.

ECC enable : Enables Error Corrceting Codes to be used in the external FIFO.

Test Mode : When set, enables reading the external FIFO. When not set, data in the FIFO will be read by the VME controller.

Configuration Register Bits: (Continued)

(Definitions and Defaults)

Reset Enables/Misc. Configuration Register

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Bit definitions	reserved						Msg. Lvl.		Rsvd.	Send Pkt on Strt	Warn on Shtdwn	JTAG	Hard Reset	SYSRST	Front Panel	Internal	
Firmware default	0	0	0	0	0	0	1	1	0	0	0	1	1	0	1	1	(0x031B)
Pow-On Cnfg. as Shpd.	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	(0x0013)

Send Pkt on Strt : Enables an INFO packet to be sent after power-up or reprogramming informing the server that the controller is ready.

Warn on Shtdwn : Enables a Warning packet to be sent informing the server of an impending shutdown/reprogram. The server should stop sending commands to the controller.

JTAG : Enables resets via the CF pin on the program PROM. Used when loading new

Hard Reset : Enables resets via the CMS/EMU Hard Reset line.

SYSRST : Enables resets via the VME backplane SYSRST signal.

Front Panel : Enables resets via the front panel push button switch.

Internal : Enables resets via a command sent in an Ethernet packet.

Msg_Lvl : Specifies the level of spontaneous messages allowed from the controller.

0: No messages will be sent from the controller.

1: Only error messages will be sent from the controller.

2: Errors and warnings will be sent from the controller.

3: Errors, warnings, and info messages will be sent from the controller.

Configuration Register Bits: (Continued)

(Definitions and Defaults)

VME Configuration Register

High Order

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Bit definitions	SYSRST in ena.	SYSRST out ena.	IH_DT_SZ		IH Req. Level		IH Req. Type		upd_irq msk	Interrupt Levels							
Firmware default	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	(0xEDFF)
Pow-On Cnfg. as Shpd.	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	(0xEDFF)

Low Order

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Bit definitions	Force SYSRS	Ena. high order	Arbiter Type		Master Req. Level		Master Req. Type		User Defs	Interrupt Handler	Location Mon.	Mask BERR	Arbiter enable	BTO enable	SYSCLK enable	Master enable	
Firmware default	0	0	0	1	1	1	0	1	0	0	0	0	1	1	1	1	(0x1D0F)
Pow-On Cnfg. as Shpd.	0	0	0	1	1	1	0	1	0	0	0	0	1	1	1	1	(0x1D0F)

SYSRST in ena. : Enable monitoring SYSRESETs on the backplane.

SYSRST out ena. : Enable SYSRESETs out to backplane.

IH_DT_SZ : Specifies the data transfer capability of the Interrupt Handler (IH).

IH Req. Level : Specifies the bus request level for the Interrupt Handler's (IH) requester (0-3).

IH Req. Type : Specifies the bus requester type for the Interrupt Handler.

0: Release On Request (ROR)
1: Release When Done (RWD)
2: Fair ROR requester.
3: Fair RWD requester.

upd_irq_msk : Update IRQ mask - restores the mask to IH_LVLS and auto resets itself to 0.

Interrupt Levels : Specifies the Interrupt ReQuest lines (IRQ's) that the IH services.

Force SYSRST : Force a SYSRESET

Ena. High order : Enable the high order bits of address and data busses.

Arbiter Type : Specifies the Arbiter type.

0: No arbitration (disabled).
1: SinGle Level arbiter (SGL), uses BR3.
2: PRIoritized arbiter (PRI).
3: Round Robin Select arbiter (RRS).

Master Req. Level : Specifies the bus request level for the VME Master's requester (0-3).

Master Req. Type : Specifies the bus requester type for the VME Master.

0: Release On Request (ROR)
1: Release When Done (RWD)
2: Fair ROR requester.
3: Fair RWD requester.

User Defs : Enables the user defined I/O buffers on J2 signals.

Interrupt Handler : Enables the Interrupt Handler. (not implemented yet)

Location Mon. : Enables the Location Monitor. (not implemented yet)

Slave enable : Enables the Slave. The slaves functions are currently only for testing purposes.

Arbiter enable : Enables the Arbiter.

BTO enable : Enables the Bus Timer. The time out value can be set by the user.

SYSCLK enable : Enables the VME SYSCLK on the backplane (16 MHz).

Master enable : Enables the VME Master.

Configuration Register Bits: (Continued)

(Definitions and Defaults)

VME Bus Timeout Register

Firmware default : 0x30D4 (200 µsec. in 16 ns units)
Pow-On Cnfg. as Shpd. : 0x30D4 (200 µsec. in 16 ns units)

VME Bus Grant Timeout Register

Firmware default : 0x0C35 (50 µsec. in 16 ns units)
Pow-On Cnfg. as Shpd. : 0x0C35 (50 µsec. in 16 ns units)

Assigning MAC Addresses

Notes on Representations:

Hexadecimal Representation:

MAC addresses are 48-bit addresses grouped into six octets. The standard representation of a MAC address is the hexadecimal representation (as defined by IEEE STD 802[1]) which is a string of six octets (in Hex) separated by hyphens, for example: AC-DE-48-00-00-80.

The ordering of the octets is as follows: octet0-octet1-octet2-octet3-octet4-octet5.

Bit-reversed Representation:

An alternative representation that is sometimes used (in the context of IEEE 802.5) is the bit-reversed representation in which the bits in each octet are reversed. In this representation the octets are separated by colons. The MAC address for the example used above in bit-reversed representation is 35:7B:12:00:00:01.

The ordering of the octets is unchanged: octet0:octet1:octet2:octet3:octet4:octet5.

Beware! Source of Confusion:

Often, MAC address are written or displayed in the hexadecimal representation but the octets are separated by colons! One example of this is the Linux /sbin/ifconfig command. In documentation and software for the Gigabit Ethernet VME Controller, the hexadecimal representation will always be intended (and should be assumed) regardless of the separater actually used.

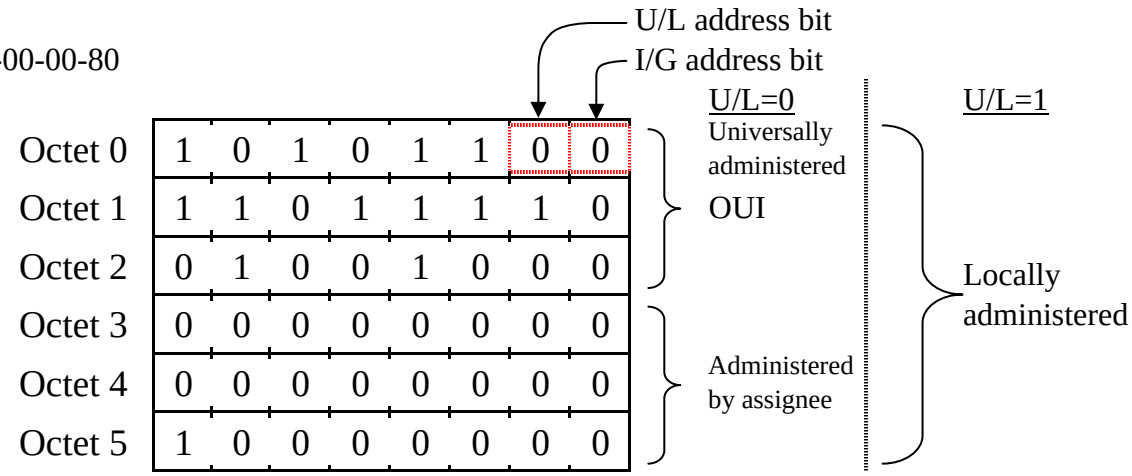
[1]IEEE Standard for Local and Metropolitan Area Networks: Overview and Architecture, The Institute of Electrical and Electronics Engineers, Inc.; 2002. (Print: ISBN 0-7381-2940-2 SH94947; PDF: ISBN 0-7381-2941-0 SS94947)

Assigning MAC Addresses (continued)

Restrictions in MAC Address Assignments:

Structure of a MAC Address:

AC-DE-48-00-00-80



I/G: Individual or Group address. LSB of octet 0.
I/G=0 - Individual address.
I/G=1 - Group address.

U/L: Universally or Locally administered. Next to LSB of octet 0.
U/L=0 - Universally administered by IEEE.
U/L=1 - Locally administered.

OUI: Organizationally Unique Identifier.

Locally Assigned Addresses:

Locally assigned address must have the U/L bit set to 1.

Valid individual MAC addresses are:
x2-xx-xx-xx-xx-xx
x6-xx-xx-xx-xx-xx
xA-xx-xx-xx-xx-xx
xE-xx-xx-xx-xx-xx

Valid MAC group addresses are:
x3-xx-xx-xx-xx-xx
x7-xx-xx-xx-xx-xx
xB-xx-xx-xx-xx-xx
xF-xx-xx-xx-xx-xx

Where the x's can be assigned any value.

Appendix A

Table of Universal Code Words

(Errors, Warnings, and Info packets)

(Packet Types 0xFF, 0xFE, and 0xFD)

Code Hex	Code Dec	Group	Mnemonic	Type	Description
0x000	0	Miscellaneous	G_No_Info	I	No information
0x001	1		CP_Un_Asgn	E	Command has not been assign to a module
0x002	2		CP_Not_Def	E	Command is not defined in this module
0x003	3		CP_No_Data	E	Expected data was not present
0x004	4		CP_Not_Exec	E	Command was not executed
0x100	256	VME Direct	VD_Dat_WtErr	E	VME Direct Data FIFO Write error (written to while full)
0x101	257		VD_Dat_AF	W	VME Direct Data FIFO Almost Full (Stop sending VME Direct Commands)
0x102	258		VD_Hdr_WtErr	E	VME Direct MAC/Hdr FIFO Write error (written to while full)
0x103	259		VD_Hdr_AF	W	VME Direct MAC/Hdr FIFO Almost Full (Stop sending VME Direct Commands)
0x110	272	VME Controller	VC_Unkn_Addr	E	Unknown VME Address
0x111	273		VC_Unkn_Dly	E	Unknown VME Delay type
0x112	274		VC_Incomp_Opt	E	Incompatible options specified in VME Control word
0x113	275		VC_RdEr_Units	E	Read error while reading number of VME Units
0x114	276		VC_RdEr_CtrlWrd	E	Read error while reading VME Control word
0x115	277		VC_RdEr_Addr	E	Read error while reading VME Address word
0x116	278		VC_RdEr_Dcnt	E	Read error while reading VME Data count word
0x117	279		VC_RdEr_Data	E	Read error while reading VME Data word
0x118	280		VC_MTEr_Fifo	E	FIFO Empty error; timedout while waiting to read
0x120	288	VME Master	VM_BERR_Slv	E	VME Bus Error initiated by slave
0x121	289		VM_BTO	E	VME Bus Time Out
0x122	290		VM_Not_Sup	E	VME command is not supported
0x130	304	VME Readback	VR_Mis_SOP	E	VME Read controller - missing Start of Packet
0x131	305		VR_Wrng_Typ	E	VME Read controller - wrong packet type seen
0x132	306		VR_Rd_TMO	E	VME Read controller - Timed out waiting for data
0x140	320	VME Interrupt Handler	VI_BERR_Slv	E	VME Bus Error initiated by slave (during interrupt)
0x141	321		VI_BTO	E	VME Bus Time Out (during interrupt)
0x142	322		VI_Msk_Chg	W	IRQ Mask has changed
0x161	353	VME Arbiter	VA_BGTO	E	VME Bus Grant Time Out

Appendix A

Table of Universal Code Words (Continued)

(Errors, Warnings, and Info packets)

(Packet Types 0xFF, 0xFE, and 0xFD)

Code Hex	Code Dec	Group	Mnemonic	Type	Description
0x200	512	External FIFO	EF_Rd_Err	E	External FIFO went empty after Read started
0x201	513		EF_MT_Err	E	External FIFO was empty when Read was requested
0x202	514		EF_Rt_Err	E	External FIFO empty or Mark not set when retransmit read was requested
0x203	515		EF_Mk_Err	E	External FIFO attempt to set Mark when almost empty
0x204	516		EF_Wrt_Err	E	External FIFO went full after Write sequence started
0x205	517		EF_FF_PAF	W	External FIFO is almost full (stop sending FIFO or VME commands)
0x206	518		EF_V_wrt_Wrn	W	VME command received while in FIFO TEST mode (Data written to FIFO)
0x207	519		EF_Rd_V_Err	E	FIFO read command received while in VME mode (no data read from FIFO)
0x208	520		EF_Mltp_Err	E	Multiple FIFO Errors
0x209	521		EF_Wrt_Wrn	W	Write command received while in VME mode (Data written to FIFO)
0x20A	522		EF_MHAF_Wrn	W	MAC/Header FIFO is almost full (Stop sending packets)
0x20B	523		EF_Drp_Err	E	Packet was dropped due to MAC/Header FIFO being full.
0x20C	524		EF_MHAMT_Inf	I	MAC/Header FIFO is almost empty.
0x20D	525		EF_AMT_Inf	I	External FIFO is almost empty.
0x210	528	Ethernet Rcv	ER_Rcv_Err	E	Ethernet Receive FIFO went empty before all packet data was read
0x230	560	JTAG	JT_Buf_AF	W	JTAG Buffer is almost full (stop sending JTAG commands)
0x231	561		JT_Buf_Ovfl	E	JTAG Buffer Overflowed (some JTAG commands are lost)
0x232	562		JT_Buf_AMT	I	JTAG Buffer is almost MT (start sending JTAG commands)
0x233	563		JT_Buf_RdErr	E	JTAG Buffer Read Error
0x234	564		JT_Unk_Cmd	E	Unknown JTAG Command
0x235	565		JT_Ver_Fail	E	PROM Verification failed
0x236	566		JT_Prg_Fail	E	PROM Programming failed

Appendix A

Table of Universal Code Words (Continued)

(Errors, Warnings, and Info packets)

(Packet Types 0xFF, 0xFE, and 0xFD)

Code Hex	Code Dec	Group	Mnemonic	Type	Description
0x240	576	Flash Controller	FL_In_AF	W	Flash Cntrl Input FIFO is almost full (stop sending Flash or Config commands)
0x241	577		FL_In_WtErr	E	Flash Cntrl Input FIFO Write Error (attempted write when full; some information lost)
0x242	578		FL_In_RdErr	E	Flash Cntrl Input FIFO Read Error (attempted read when empty; data invalid)
0x243	579		FL_TRDS_WtErr	E	Flash Cntrl Total ReaDS FIFO Write Error (attempted write when full; some information lost)
0x244	580		FL_TRDS_RdErr	E	Flash Cntrl Total ReaDS FIFO Read Error (attempted read when empty; data invalid)
0x245	581		FL_PgRd_WtErr	E	Flash Cntrl Page/Read FIFO Write Error (attempted write when full; some information lost)
0x246	582		FL_PgRd_RdErr	E	Flash Cntrl Page/Read FIFO Read Error (attempted read when empty; data invalid)
0x247	583		FL_ADFF_WtErr	E	Flash Cntrl Address FIFO Write Error (attempted write when full; some information lost)
0x248	584		FL_ADFF_RdErr	E	Flash Cntrl Address FIFO Read Error (attempted read when empty; data invalid)
0x250	592	Config	CF_Mltp_Flsh	E	Multiple errors from Flash Controller (see following data word for error bits).
0x251	593		CF_Crptd_Dat	E	Corrupted data from Flash Controller (uncorrected bit errors).
0x252	594		CF_Bit_Errs	W	Bit errors in data from Flash Controller were found and corrected.
0x260	608	Reset Hndlr.	RH_xxx_xxx	W	
0x270	624	Start-up Shutdown	SS_Rld_Pndg	W	Controller is shuting down to reload firmware
0x271	625		SS_Sys_Up	I	Controller system is back up