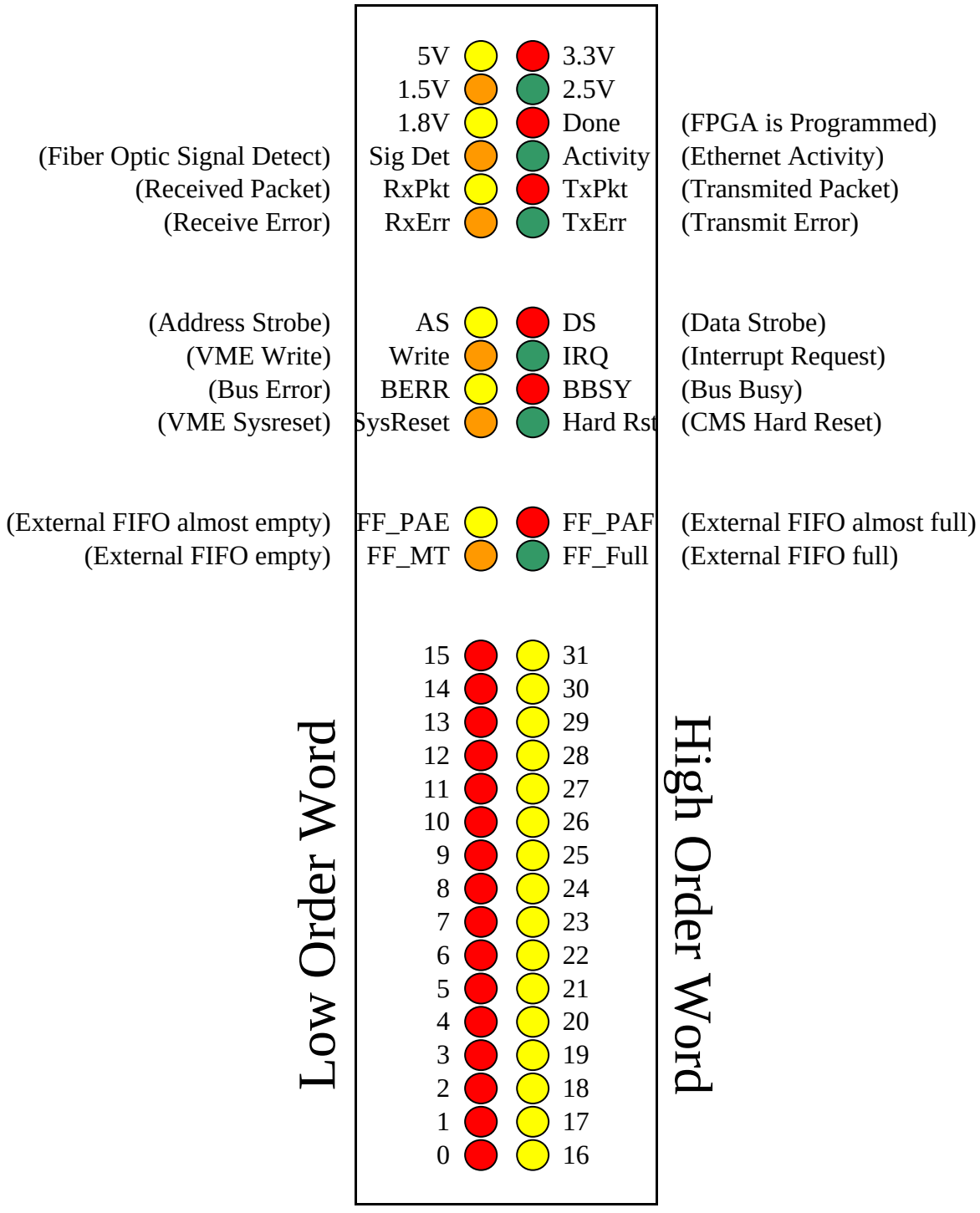
Front Panel LED Signal Assignments

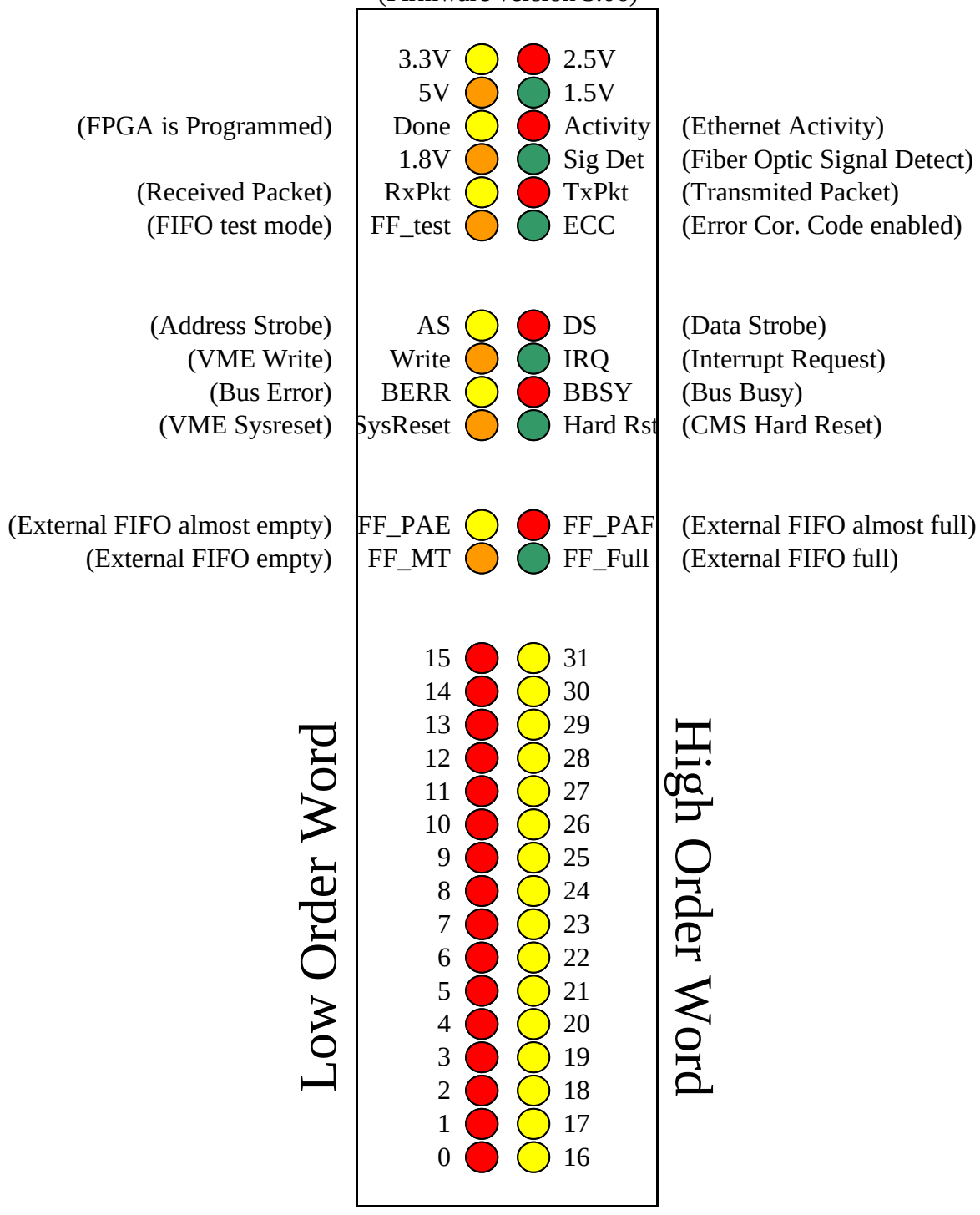
Production VCC's



Front Panel LED Signal Assignments

Pre-Production VCC's

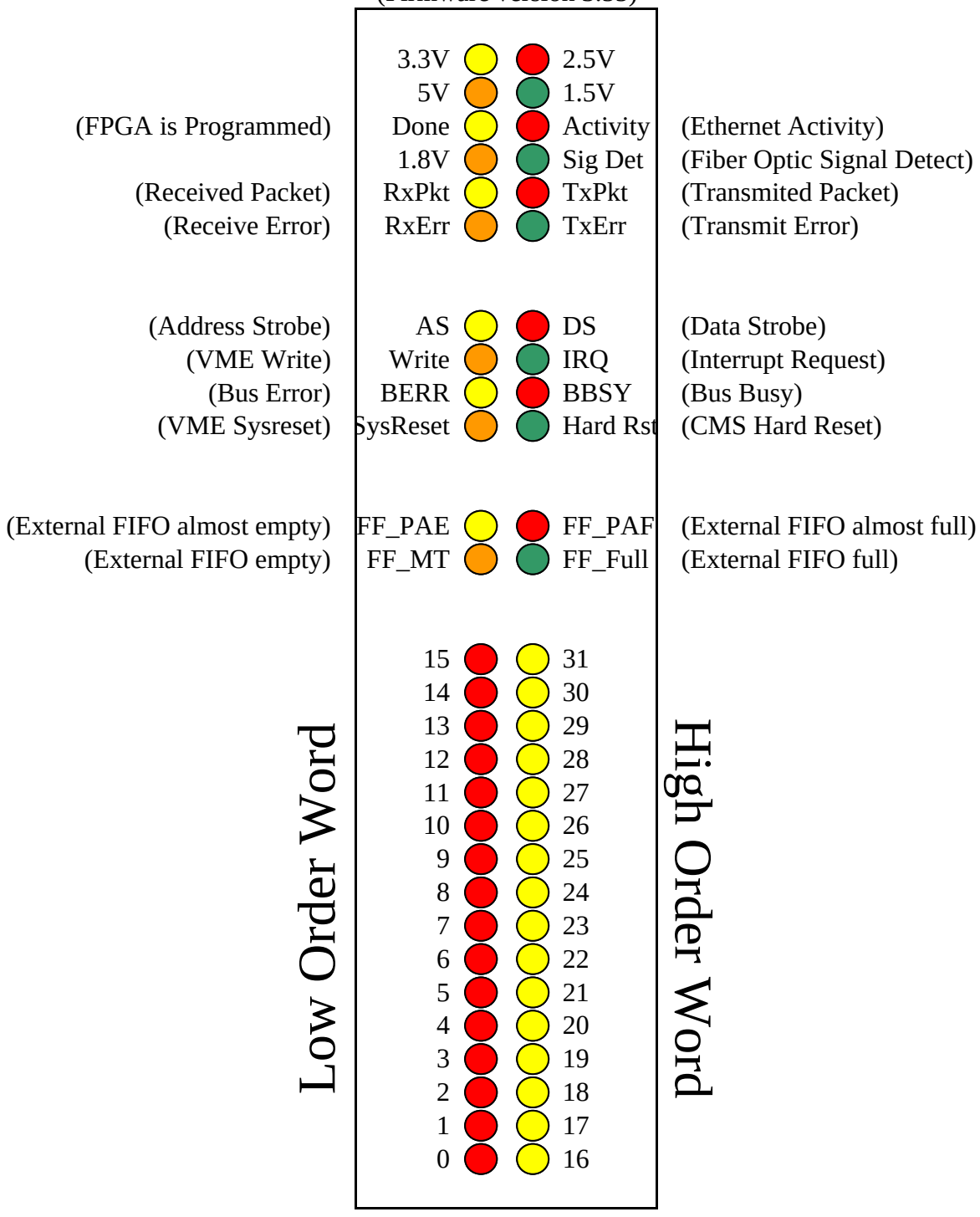
(Firmware version 3.06)



Front Panel LED Signal Assignments

Pre-Production VCC's

(Firmware version 3.55)



Switch Settings

LED Switch: (Switch 1)

LED Mode	Display Assignment
0	User register (user defined 32 bits)
1	Transmit (right half) and Receive (left half) packet count (16 bits each)
2	Full received count (32 bits)
3	Full transmit count (32 bits)
4	TXStatus (right half) and RXStatus (left half) (16 bits each)
default	Full received count (32 bits)
E	Transmit error count (32 bits)
F	Dropped packet count (32 bits)

Mode Switch: (Switch 2)

Version	Switch function
Prior to 3.06	Fixed function: Switch setting controlled the Ethernet options according to the table on the left below.
3.06	Ethernet options are controlled either by the switch or by Ether_Cnfg CR according to the value of Ether_Cnfg[7] (Switch Control bit). If Switch Control is set, Switch 2 controls the Ethernet options the same as prior to version 3.06.
3.55	Switch 2 now selects groups of signals to be directed to the Test Ports for logic analyzer use (see the table on the right below). Ethernet options are controlled exclusively by the configuration register.

Prior to rev. 3.06
or rev. 3.06 with Ether_Cnfg[7] set.

Mode	Pass-Through	Promiscuous	Protocol Enabled	Carrier Extend
0	-	-	X	-
1	-	-	-	-
2	X	-	-	-
3	X	X	-	-
4	-	X	X	-
5	-	-	X	X
default	-	-	X	-

Revision 3.55

Mode	Signal Groups
0	VME Ctrl.(input) and VME Master (busy)
1	VME Ctrl.(output) and VME Master (internal)
2	VME Ctrl.(output) and VME Master (busy)
3	VME Ctrl.(handshake) and VME Master (berr)
4	Interrupt Handler
5	Requester, Arbiter, and VME Master
6	Master requester and VME Master
7	IH requester, Arbiter. and VME Master
8	IH requester and VME Master
9	VME Master (internal)

Status Word Definitions

RXStatus Register:

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Gd_Fr	Gd_CRC	Bad_CRC	No_CRC	FF_Full	FF_MT	Len_OK	Ovr_Max	Loc_Mtch	BCast_Mtch	MCast_Mtch	0	Error	State		

Receive Status Bit Definitions

Mnemonic	Meaning
Gd_Fr	Good Frame: Packet accepted.
Gd_CRC	Packet CRC matched calculated CRC.
Bad_CRC	Packet CRC did not match calculated CRC.
No_CRC	No CRC check was seen.
FF_Full	Frame FIFO is Full.
FF_MT	Frame FIFO is Empty.
Len_OK	Packet length is matched embedded length.
Ovr_Max	Packet exceeds the maximum byte count.
Local_Match	MAC address matches the devices own address.
BCast_Match	MAC address matches the MAC broadcast address.
MCast_Match	MAC address matches the multicast address.
Error	Error occurred while receiving packet.
State	State of MAC processor state machine at time of error.

MAC Processor State Definitions

State	Operation
0	Waiting for start of packet.
1	Preamble
2	MAC Destination
3	MAC Source
4	Storing length
5	Receiving payload
6	Update statistics
7	Wait for idle.

Status Word Definitions (continued)

TXStatus Register:

Prior to revision 3.06

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TX_Err	TBErr	TKErr	TMErr	0	0	0	TX_Proc	PB_Full	PB_AF	0	PB_MT	Prio_PB_Full	Prio_PB_AF	0	Prio_PB_MT

Revision 3.06 and later

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TX_Err	TBErr	TKErr	TMErr	TX_Proc	Norm_PB_Full	Norm_PB_AF	Norm_PB_MT	0	Prio_PB_Full	Prio_PB_AF	Prio_PB_MT	0	Spont_PB_Full	Spont_PB_AF	Spont_PB_MT

Transmit Status Bit Definitions

Mnemonic	Meaning
TX_Err	Transmit error (OR or TBErr, TKErr, and TMErr).
TBErr	Rocket IO transmit buffer error.
TKErr	Invalid K character.
TMErr	Error in the MAC destination.
TX_Proc	Transmition of a packet is in progress.
Norm_PB_Full	Normal Packet Builder FIFO is full.
Norm_PB_AF	Normal Packet Builder FIFO is almost full.
Norm_PB_MT	Normal Packet Builder FIFO is empty.
Prio_PB_Full	Prioity Packet Builder FIFO is full.
Prio_PB_AF	Prioity Packet Builder FIFO is almost full.
Prio_PB_MT	Prioity Packet Builder FIFO is empty.
Spont_PB_Full	Spontaneous Packet Builder FIFO is full.
Spont_PB_AF	Spontaneous Packet Builder FIFO is almost full.
Spont_PB_MT	Spontaneous Packet Builder FIFO is empty.